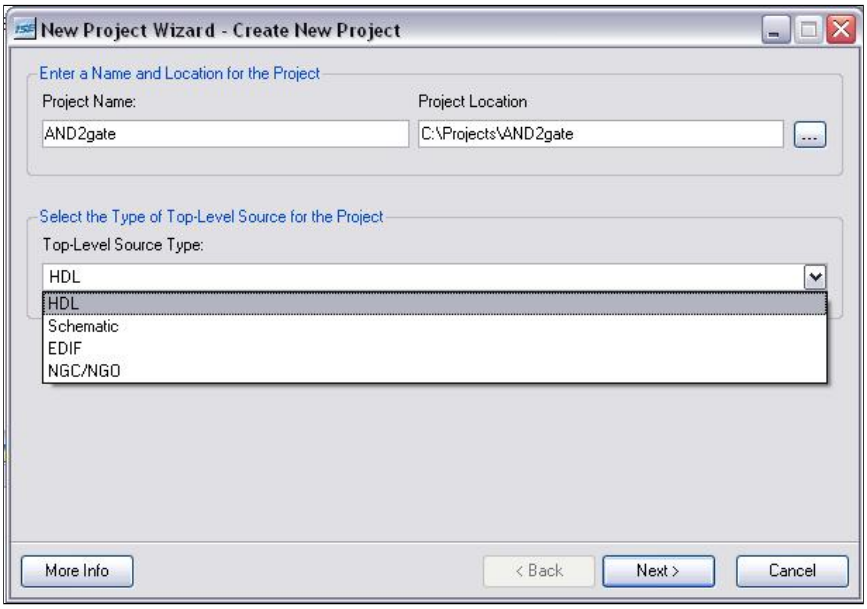
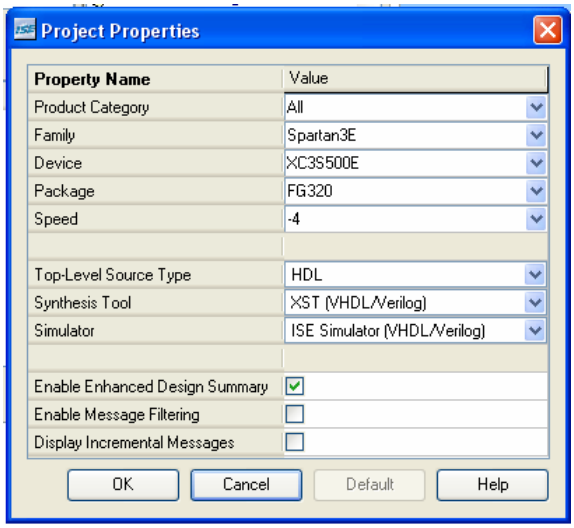
Xilinx ISE 8.1 Simulation Tutorial

1. Start Xilinx ISE Project Navigator
2. Create a new project
   - Click on *File*, then choose *New Project* on the drop down menu
   - Enter your project name, in this case the project is called “AND2gate”
   - Choose your project location, this project is stored at “Z:\Projects\AND2gate”
   - Choose *HDL* as the source type from the *Top-Level Source Type* menu.
   - Click *Next* button



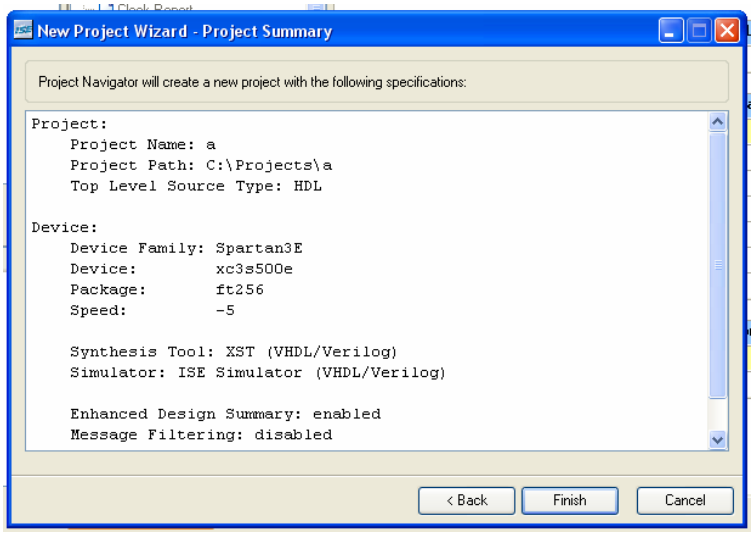
3. You will be asked to select the hardware and design flow for this project.
   - For *Family*, choose *Spartan3E*
   - For *Device*, choose *XC3S500E*
   - For *Package*, choose *FG320*
   - For *Speed*, choose *-4*
   - For *Simulator*, choose *ISE Simulator (VHDL/Verilog)*
   - Click *Next* button



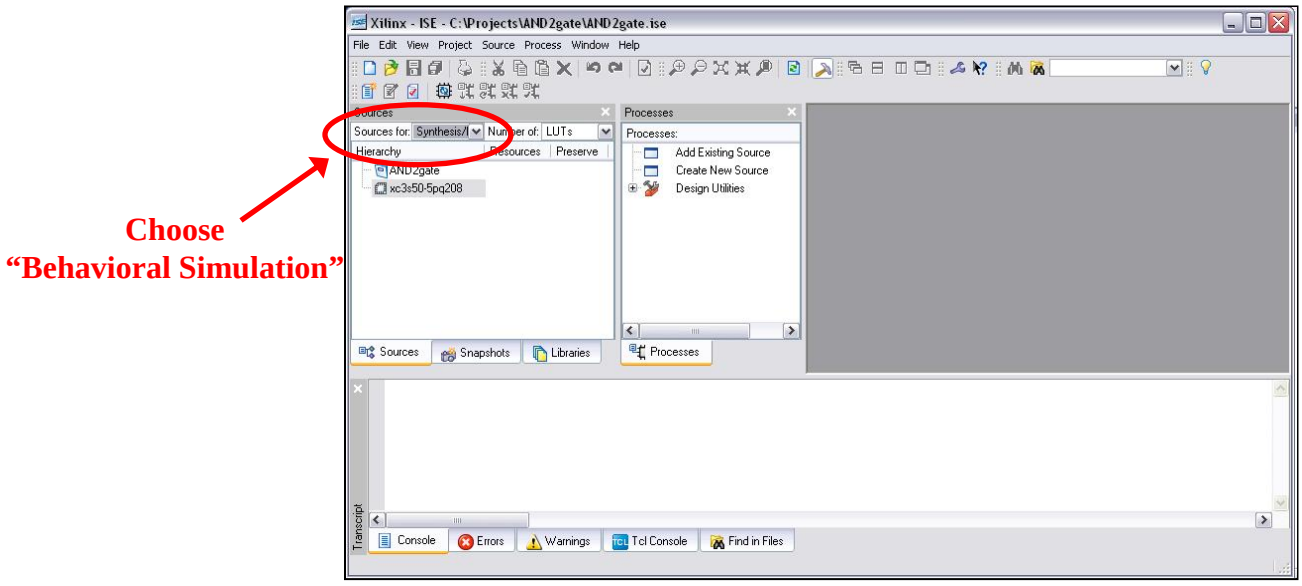
4. Next you are asked if you want to create new source files. We'll add source files later so just click on the *Next* button.

5. You are asked if you want to add existing source files. Since we have a new project we don't have any existing files. Additionally, if you did have pre-existing files, you can also add these to the project later. Click on the *Next* button.

6. A project summary will appear. Click on the *Finish* button.

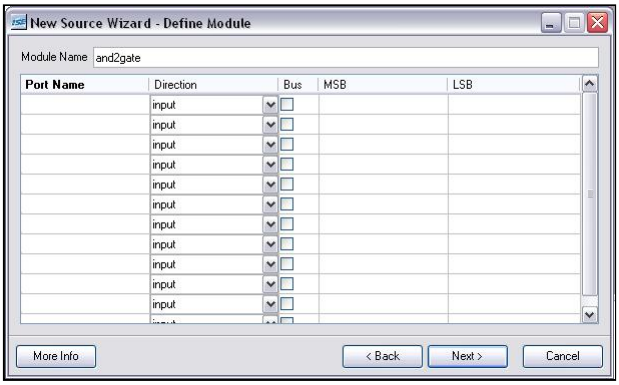


7. You now have a project by the name of “AND2gate”. Next you want to specify the files in this project are for behavioral simulation.
   - Click on the *Sources for:* drop down menu, choose *Behavioral Simulation*

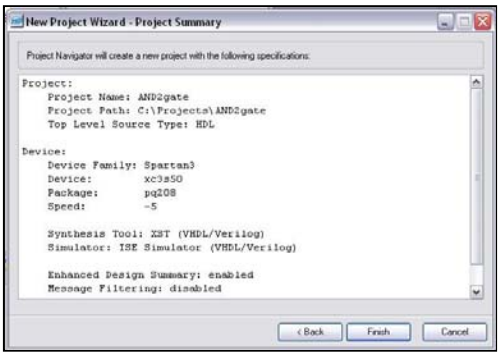


8. Now we want to add a new file to our project.
   - Click on *Project*, choose *New Source*
   - Choose *Verilog Module* as the file type
   - In the *File name:* box enter the desired file name, in this case the file is named “and2gate.v”
   - Click on the *Next* button

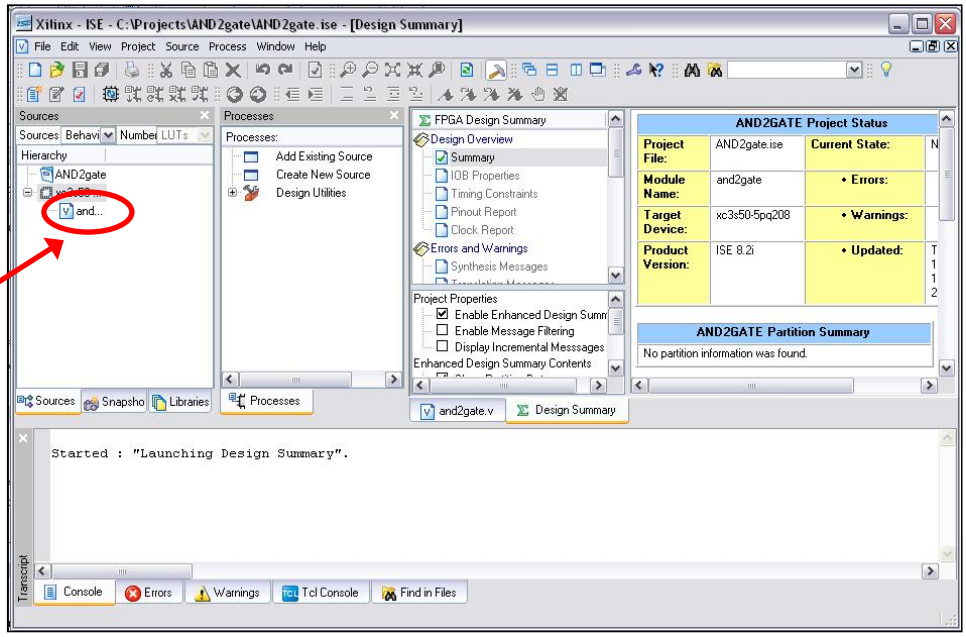
9. You will be asked for the module’s port names/types. You can skip this step and click on the *Next* button.



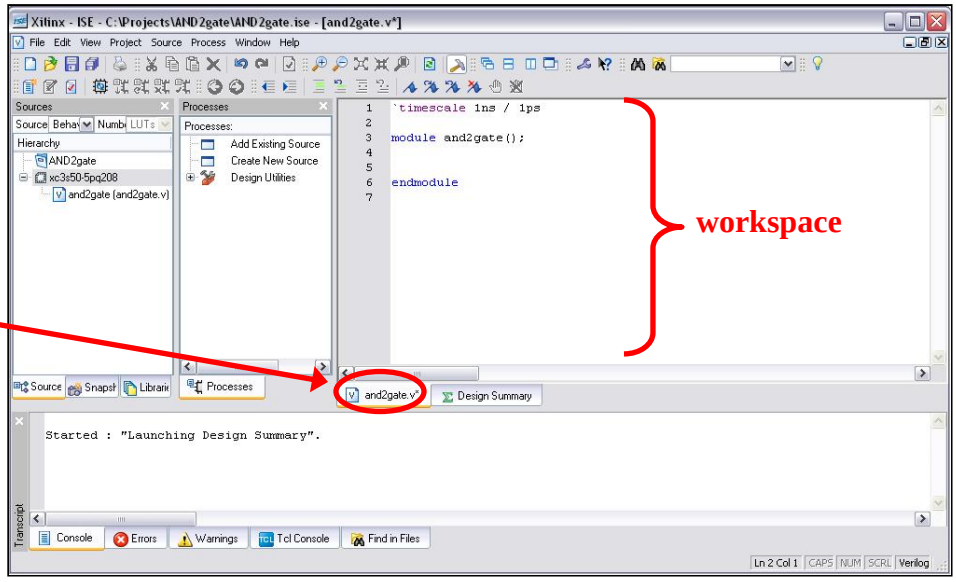
10. A project summary will appear. Click on the *Finish* button.



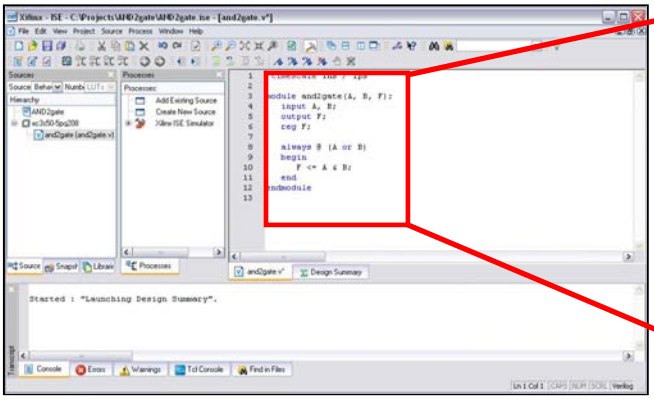
11. The "and2gate.v" file has been added to your project.



12. Click on the and2gate.v tab to show the file contents. You are now ready to specify the and2gate module's functionality.

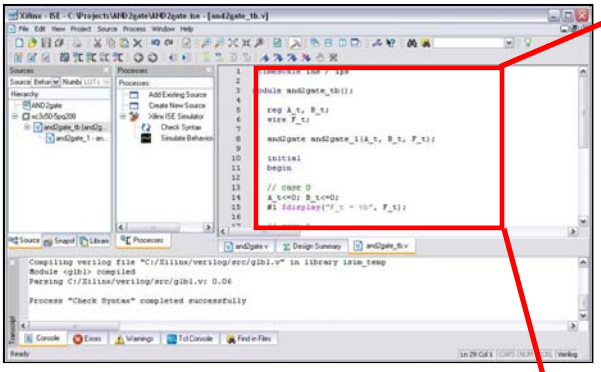


13. Notice that the ISE has already entered a couple of lines of code for us.
    - The line "`timescale 1ns/ 1ps" is located at the top of the file. The Verilog language uses dimensionless time units, and these time units are mapped to "real" time units within the simulator. `timescale is used to map to the "real" time values using the statement `timescale <time1> / <time2>, where <time1> indicates the time units associated with the #delay values, and the <time2> indicates the minimum step time used by the simulator.
    - The and2gate module is also declared using "module and2gate();" and "endmodule", but the ports are left for us to define.
    - We finish specifying the functionality of the and2gate module as shown below.



```
`timescale 1ns / 1ps

module and2gate(A, B, F);
        input A, B;
        output F;
        reg F;

        always @ (A or B)
        begin
                F <= A & B;
        end
endmodule
```

14. We also want to add a test bench and again follow Steps 8 – 11 to add "and2gate_tb". Then we add the functionality of the testbench module as shown below.

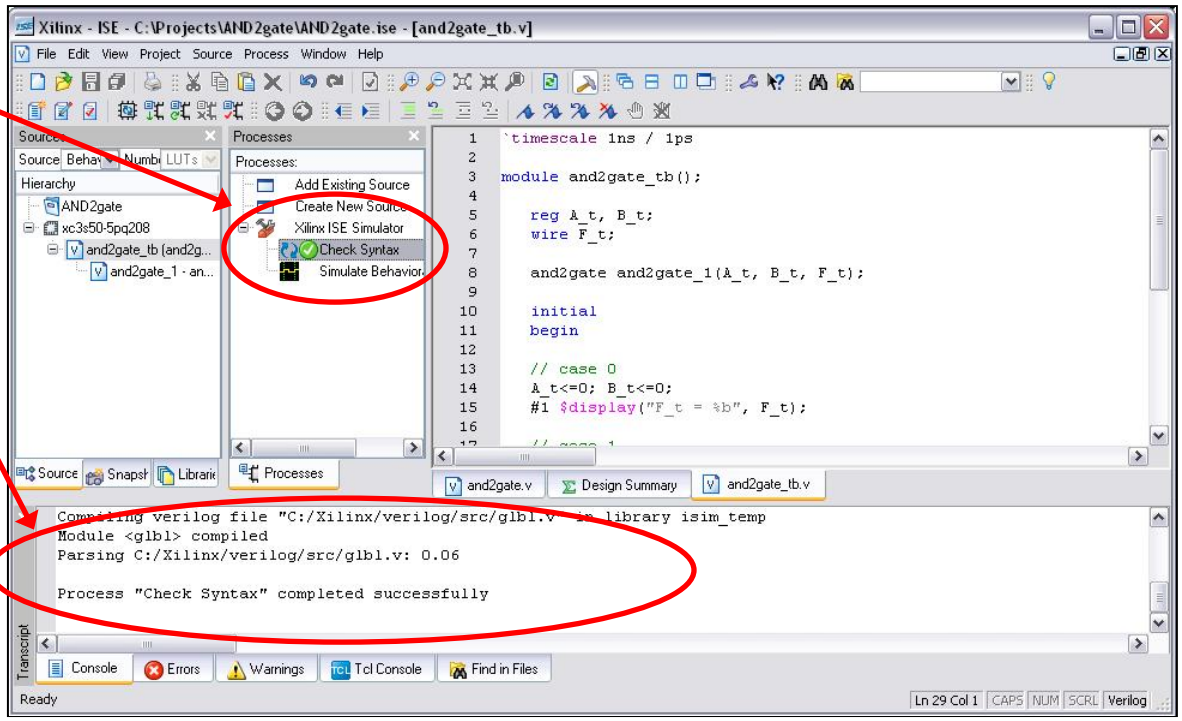


```
`timescale 1ns / 1ps

module and2gate_tb();
  reg A_t, B_t;
  wire F_t;

  and2gate and2gate_1(A_t, B_t, F_t);

  initial
  begin

    // case 0
    A_t<=0; B_t<=0;
    #1 $display("F_t = %b", F_t);

    // case 1
    A_t<=0; B_t<=1;
    #1 $display("F_t = %b", F_t);

    // case 2
    A_t<=1; B_t<=0;
    #1 $display("F_t = %b", F_t);

    // case 3
    A_t<=1; B_t<=1;
    #1 $display("F_t = %b", F_t);

  end
endmodule
```

15. After saving both “and2gate.v” and “and2gate_tb.v”, we want to check the syntax of both files.
    - Expand the *Xilinx ISE Simulator* menu, double click on *Check Syntax*
    - If the syntax was correct, a checkmark appears beside the *Check Syntax* menu
    - If the syntax was incorrect, the window at the bottom will list the individual errors.

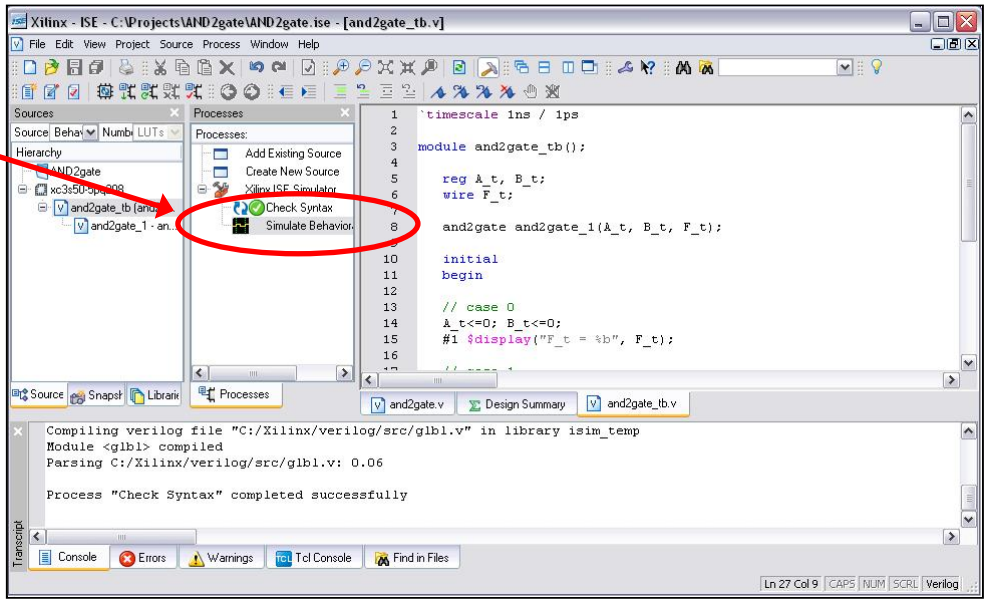
Expand Xilinx ISE Simulator menu, double click on Check Syntax

Any errors will be listed here

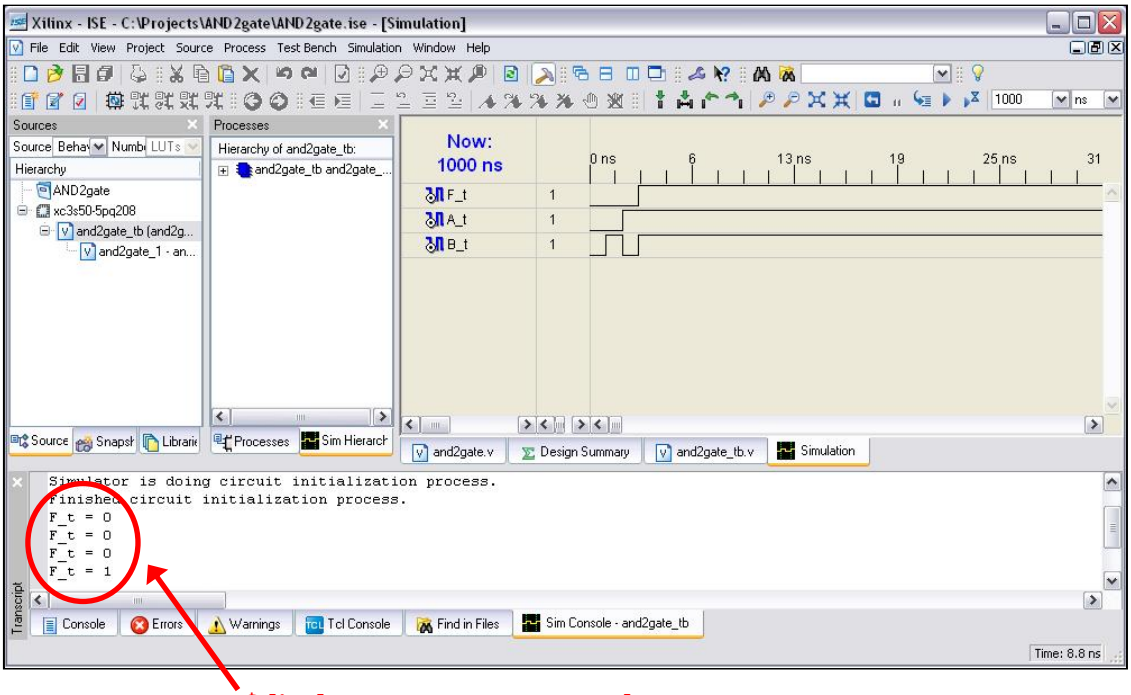


16. Now it’s time to simulate the design.
    - Double-click on the *Simulate Behavior* icon

Double-click on “Simulate Behavior”



17. The simulation waveforms appear and we can check the and2gate module's functionality. Further, the $display statements included in the testbench appear in the lower window.



$display statements appear here